REMARKS

The present application was filed on February 16, 2001 with claims 1 through 23. Claims 1 through 23 are presently pending in the above-identified patent application.

In the Office Action, the Examiner rejected claims 1, 6, 8, and 14 under 35 U.S.C. §102(e) as being anticipated by Gulick (United States Patent Number 6,601,178), rejected claims 2, 7, 11, 15-17, and 19-23 under 35 U.S.C. §103(a) as being unpatentable over Gulick in view of Kanuma (United States Patent Number 4,587,445), rejected claim 3 under 35 U.S.C. §103(a) as being unpatentable over Gulick in view of Azarya et al. (United States Patent Number 5,978,578), rejected claim 18 under 35 U.S.C. §103(a) as being unpatentable over Gulick in view of Kanuma, and further in view of Azarya et al., and rejected claims 4, 5, 12, and 13 under 35 U.S.C. §103(a) as being unpatentable over Gulick. The Examiner also rejected claim 9 under 35 U.S.C. §103(a) as being unpatentable over Gulick in view of Buch (United States Patent Number 5,230,067) and rejected claim 10 under 35 U.S.C. §103(a) as being unpatentable over Gulick in view of Buch, and further in view of Albrecht et al. (United States Patent Number 5,281,822).

The present invention is directed to a method and apparatus for transferring multi-source/multi-sink control signals using a differential signaling technique. An "active" state is transferred on a multi-source/multi-sink control signal network by inverting the previous voltage level, and an "inactive state" is transferred by maintaining the previous level. A change in the voltage level associated with a given control signal indicates that at least one node on an SoC device is asserting the corresponding control signal. In order to detect a change in the signal state from a previous cycle, each node includes a memory element, such as a latch, for maintaining the previous state. In this manner, a voltage level from the next interval can be compared to the recorded state to detect a change of state indicating an assertion of the control signal by another node. Thus, a given control signal is asserted whenever the state of the signal at the end of the previous cycle is different from the state of the signal at the end of the proceeding cycle. In one exemplary implementation, the asserted control signal is applied to an exclusive-OR gate together with the current value on the control signal wire to thereby cause a transition indicating an assertion of the control signal.

Independent Claims 1, 8 and 16

Independent claims 1, 8, and 16 were rejected under 35 U.S.C. §102(e) as being anticipated by Gulick.

Regarding claim 1, the Examiner asserts that Gulick teaches maintaining said voltage level of said control signal from the previous time interval to indicate a second signal state (col. 10, lines 19-26; the maintaining of voltage level is indicative of remaining in the current power consumption state).

Applicants note that in the text cited by the Examiner, Gulick teaches "changing the voltage level of a control line of the bus from *a voltage level at which the control line is maintained during the reduced power consumption state* to a *different voltage level to indicate the bus is being brought to the normal power consumption state.*" (Emphasis added.) Gulick defines two power consumption states: a first state defined as a reduced power consumption state and a second state defined as a normal power consumption state. The first state is indicated by "a voltage level" and the second state is indicated by a "different voltage level." Thus, both states are detected by monitoring for a *particular voltage level, not monitoring for a change in the voltage level.* In contrast to the present invention, Gulick teaches that a change in voltage level is indicative of a change in state, and ***not*** indicative of a particular state. Independent claim 1 requires ***adjusting*** *a voltage level* of said control signal from a previous time interval to indicate a ***first signal state***. Independent claims 8 and 16 require detecting a ***first signal state*** for said control signal if a *voltage level* from a previous time interval ***is adjusted***.

Thus, Gulick does not disclose or suggest adjusting a voltage level of said control signal from a previous time interval to indicate a first signal state, as required by independent claim 1, and does not disclose or suggest detecting a first signal state for said control signal if a voltage level from a previous time interval is adjusted, as required by independent claims 8 and 16.

In addition, although Gulick clearly defines two states as described above, the Examiner seems to be interpreting Gulick as teaching that the control line has two "states:" a "first state" indicated by an adjustment of the voltage level that represents a "change in power consumption state" and a "second state" indicated by maintaining a voltage level representing "remaining in the current power consumption state." A state,

however, is defined by a discrete value *during a time interval.* Thus, it is not proper to define a state as representing a "change in power consumption state." If, for sake of argument, a state could be defined as a change of state by another state variable, Applicants would note that the time intervals disclosed by Gulick are defined by a change of the voltage level of the control signal, and thus every time interval corresponds to a change in the state of the power consumption. There are no transitions between time intervals that correspond to maintaining the same state of power consumption.

Additional Cited References

Kanuma was also cited by the Examiner for disclosing a memory element for maintaining a voltage level from a previous time interval.

Applicants note that Kanuma discloses both data signals (including T1..TN, L1..L(N+1), R1..RN, and IN1..IN3) and a control signal (the output of the Majority Circuit 26). The data signals are utilized for transmitting data or information and *not* control signals. Independent claims 1, 8, and 16 are directed to transmitting a control signal.

Regarding the control signal taught by Kanuma, Applicants note that Kanuma teaches a first signal state (logic-0) to indicate that the data signals T1..TN should not be inverted and a second signal state (logic-1) to indicate that the data signals T1..TN should be inverted. The first and second signal states taught by Kanuma are indicated by a **fixed** high voltage (logic-1) and low voltage (logic-0), respectively. Thus, each signal state taught by Kanuma is indicated by a *specific voltage level.* Independent claim 1 requires ***adjusting*** *a voltage level of said control signal* ***from a previous time interval*** to indicate a first signal state. Independent claims 8 and 16 require detecting a first signal state for said control signal if a *voltage level* ***from a previous time interval is adjusted.***

Thus, Kanuma does not disclose or suggest adjusting a voltage level of said control signal from a previous time interval to indicate a first signal state, as required by independent claim 1, and does not disclose or suggest detecting a first signal state for said control signal if a voltage level from a previous time interval is adjusted, as required by independent claims 8 and 16.

Azarya was also cited by the Examiner for disclosing the step of ensuring that only a single node connected to the bus can assert a control signal in a given time interval (col. 13, lines 54-56). Applicants note that Azarya is directed to a "control automation system for enabling I/O boards to access communication networks for receiving and transmitting real time control information over a communication network." (See, Abstract.) Azarya does not disclose adjusting a voltage level from a previous time interval to indicate a first signal state of a control signal.

Thus, Azarya does not disclose or suggest adjusting a voltage level of said control signal from a previous time interval to indicate a first signal state, as required by independent claim 1, and does not disclose or suggest detecting a first signal state for said control signal if a voltage level from a previous time interval is adjusted, as required by independent claims 8 and 16.

Buch was also cited by the Examiner for disclosing the step of maintaining the control signal value at the voltage level from the previous time interval when no node drives the bus (col. 5, lines 64-68; col. 6, lines 1-5). Applicants note that Buch is directed to a latch circuit that "latches data states on the data bus after the bus has been driven to a desired state by a system driver node." (See, Abstract.) Buch does not disclose adjusting a voltage level from a previous time interval to indicate a first signal state of a control signal.

Thus, Buch does not disclose or suggest adjusting a voltage level of said control signal from a previous time interval to indicate a first signal state, as required by independent claim 1, and does not disclose or suggest detecting a first signal state for said control signal if a voltage level from a previous time interval is adjusted, as required by independent claims 8 and 16.

Albrecht was also cited by the Examiner for disclosing a field plate that prevents leakage and cross-coupling (col. 17, lines 37-40). Applicants note that Albrecht is directed to "a neuron detector for use in high energy flux environments." (See, Abstract.) Albrecht does not disclose adjusting a voltage level from a previous time interval to indicate a first signal state of a control signal.

Thus, Albrect does not disclose or suggest adjusting a voltage level of said control signal from a previous time interval to indicate a first signal state, as required by

independent claim 1, and does not disclose or suggest detecting a first signal state for said control signal if a voltage level from a previous time interval is adjusted, as required by independent claims 8 and 16.

Dependent Claims 2-7, 9-15 and 17-23

Dependent claims 6 and 14 were rejected under 35 U.S.C. §102(e) as being anticipated by Gulick, claims 2, 7, 11, 15, 17, and 19-23 were rejected under 35 U.S.C. §103(a) as being unpatentable over Gulick in view of Kanuma, claim 3 was rejected under 35 U.S.C. §103(a) as being unpatentable over Gulick in view of Azarya et al., claim 18 was rejected under 35 U.S.C. §103(a) as being unpatentable over Gulick in view of Kanuma, and further in view of Azarya et al., claims 4, 5, 12, and 13 were rejected under 35 U.S.C. §103(a) as being unpatentable over Gulick, claim 9 was rejected under 35 U.S.C. §103(a) as being unpatentable over Gulick in view of Buch, and claim 10 was rejected under 35 U.S.C. §103(a) as being unpatentable over Gulick in view of Buch, and further in view of Albrecht et al.

Claims 2-7, 9-15 and 17-23 are dependent on claims 1, 8, and 16, respectively, and are therefore patentably distinguished over Gulick, Kanuma, Azarya et al., Buch, and Albrecht et al. (alone or in any combination) because of their dependency from independent claims 1, 8, and 16 for the reasons set forth above, as well as other elements these claims add in combination to their base claim.

All of the pending claims, i.e., claims 1-23, are in condition for allowance and such favorable action is earnestly solicited.

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Examiner is invited to contact the undersigned at the telephone number indicated below.

The Examiner's attention to this matter is appreciated.

Respectfully submitted,

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